Tightly-Coupled FPGA Cluster with TERASIC DE5-NET boards

Custom Computing Framework for Real Applications

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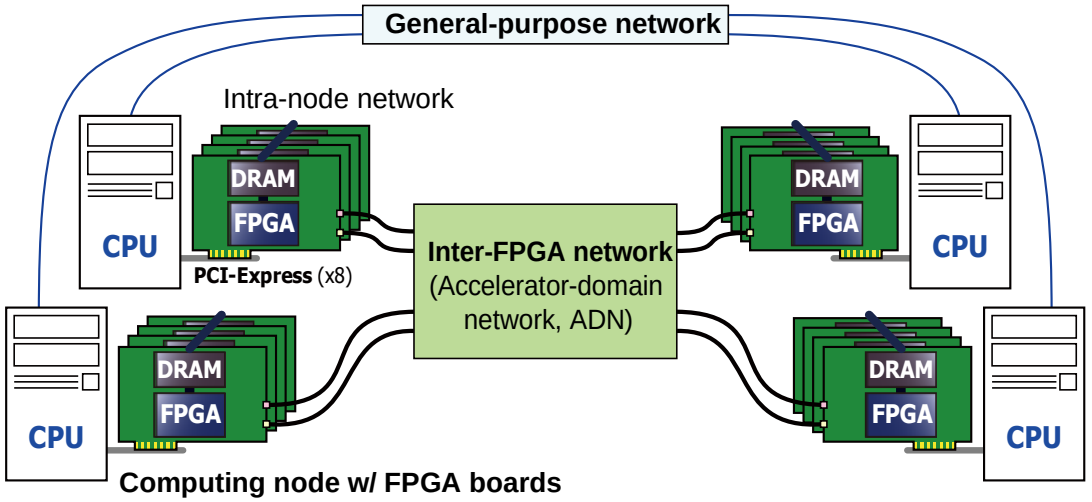
Why Tightly-Coupled FPGA Cluster?

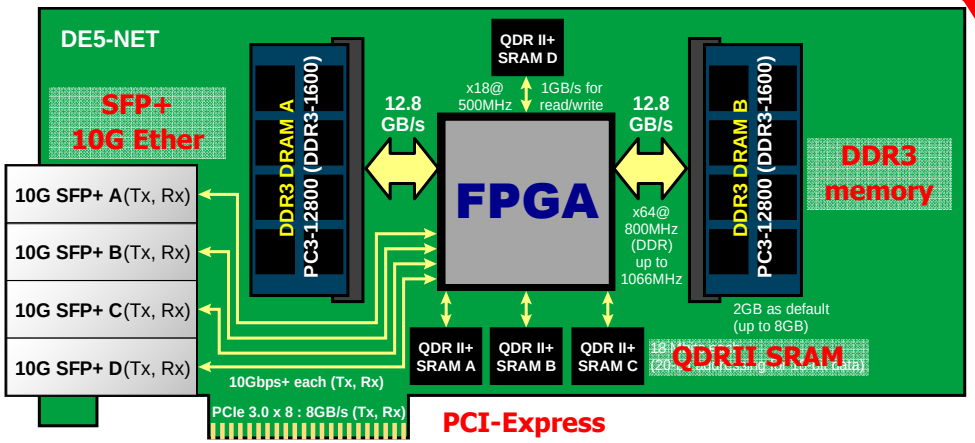
- **Low-power and scalable custom computing with FPGAs**
  - ✓ Low-power : dedicated data-paths, memory systems, networks on FPGAs
  - ✓ Scalable : low-latency HW-to-HW direct communication/synchronization via **accelerator-domain network: ADN**
- **Testbed for development and product run of "real" applications**
  - ✓ Qsys-based hardware framework on FPGA
  - ✓ Linux driver, API, FPGA-class library for software development
  - ✓ Researches for compilers, tools, and applications
  - ✓ Experiences with running an actual system (trouble shooting, etc.)



Architecture of tightly-coupled FPGA cluster

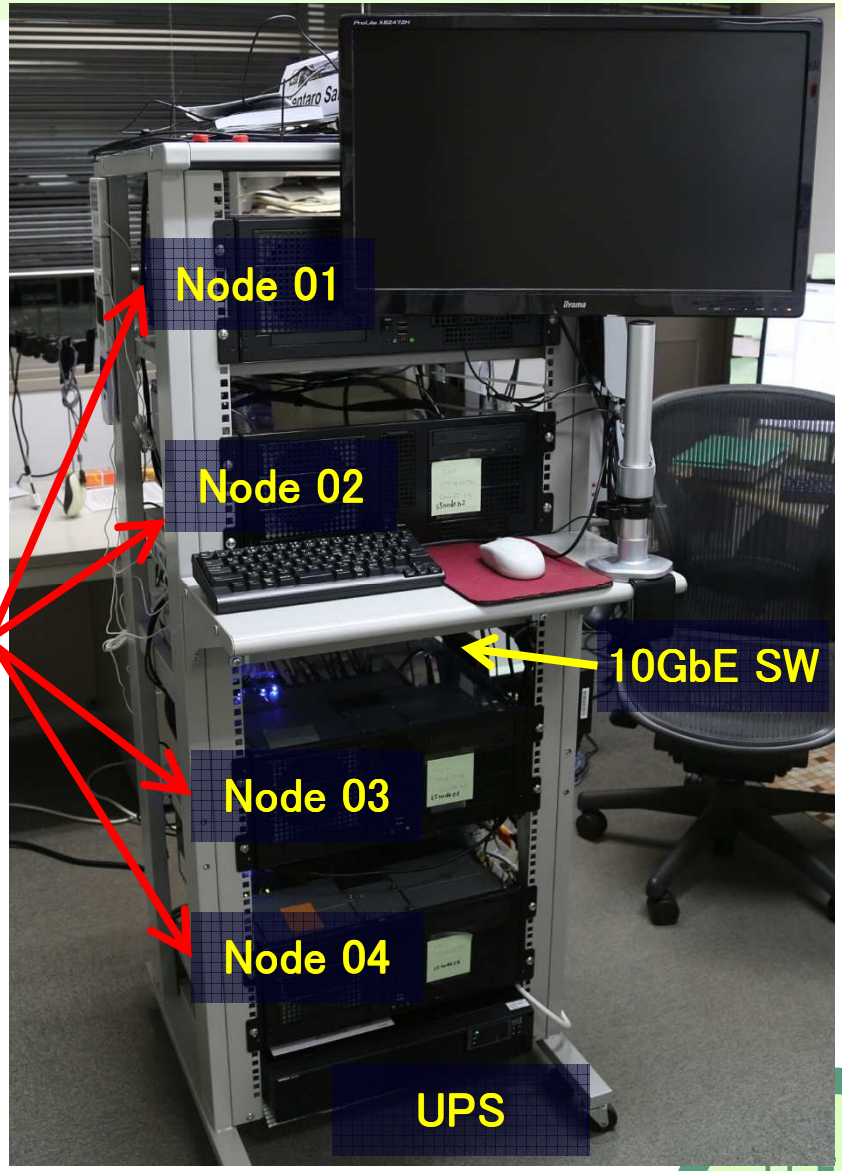
Tightly-Coupled FPGA Cluster Overview

- **System configuration**
  - ✓ 4 x host PCs
  - ✓ 4 x FPGAs / PC
  - ✓ 4 x 10G SFP+ ports / FPGA
- **Implementation**
  - ✓ Linux on nodes
  - ✓ Qsys framework on FPGAs

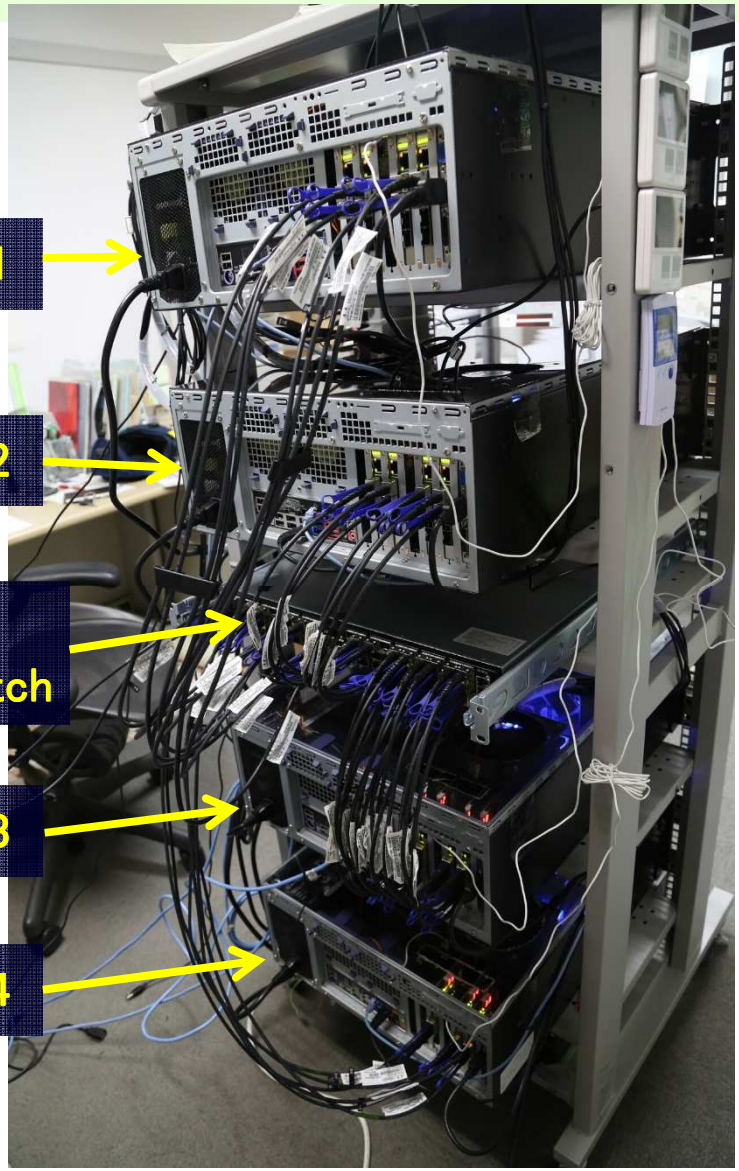


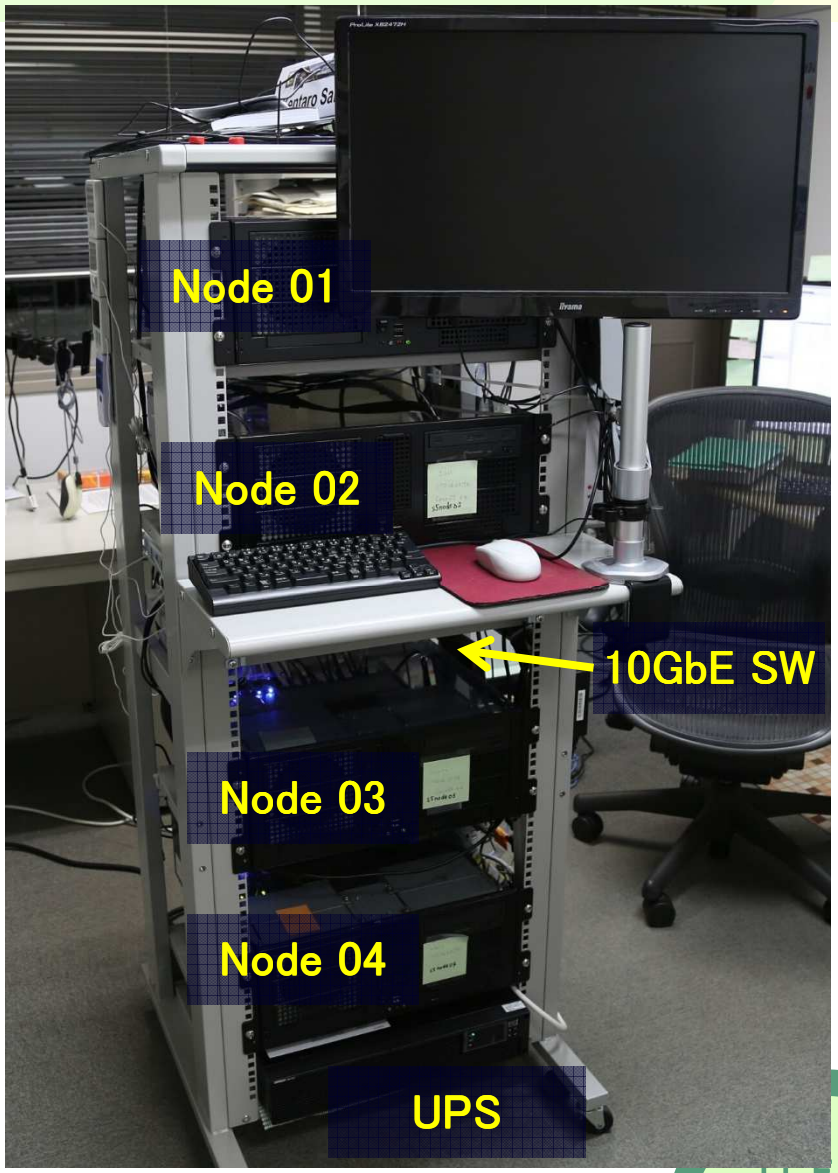
FPGA board (Stratix V)

x 4 each

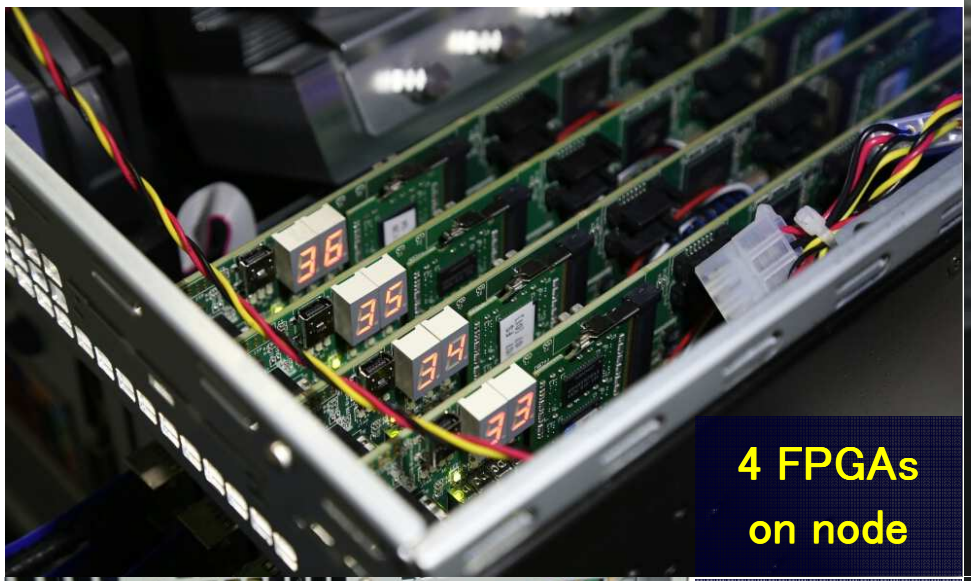


Front and Back

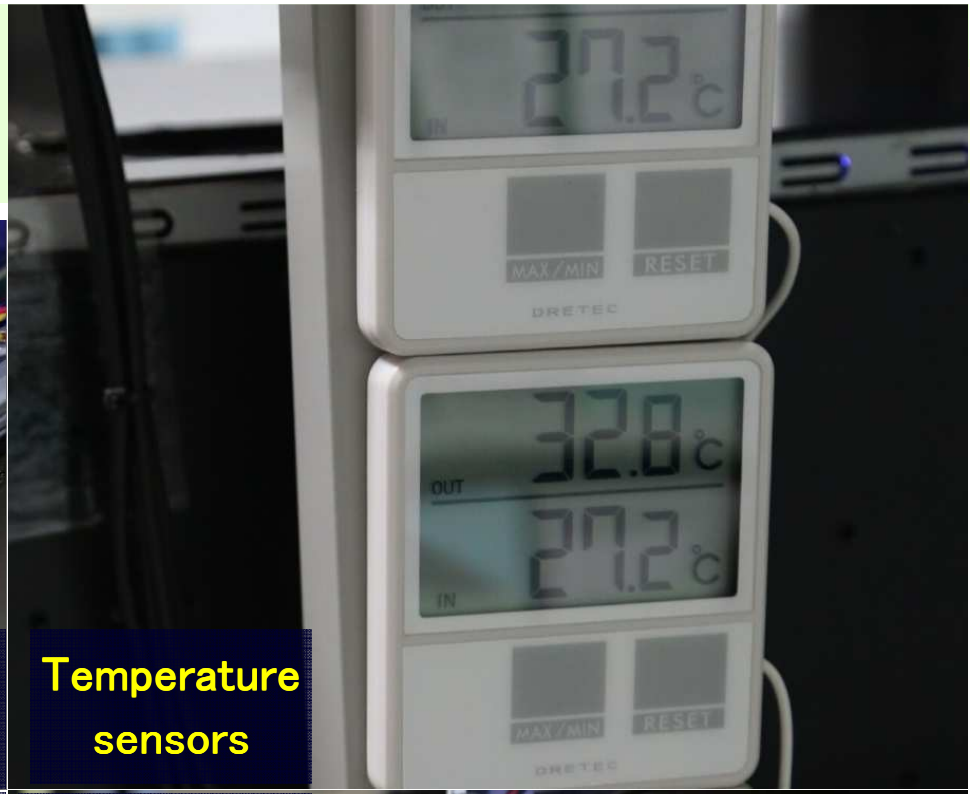




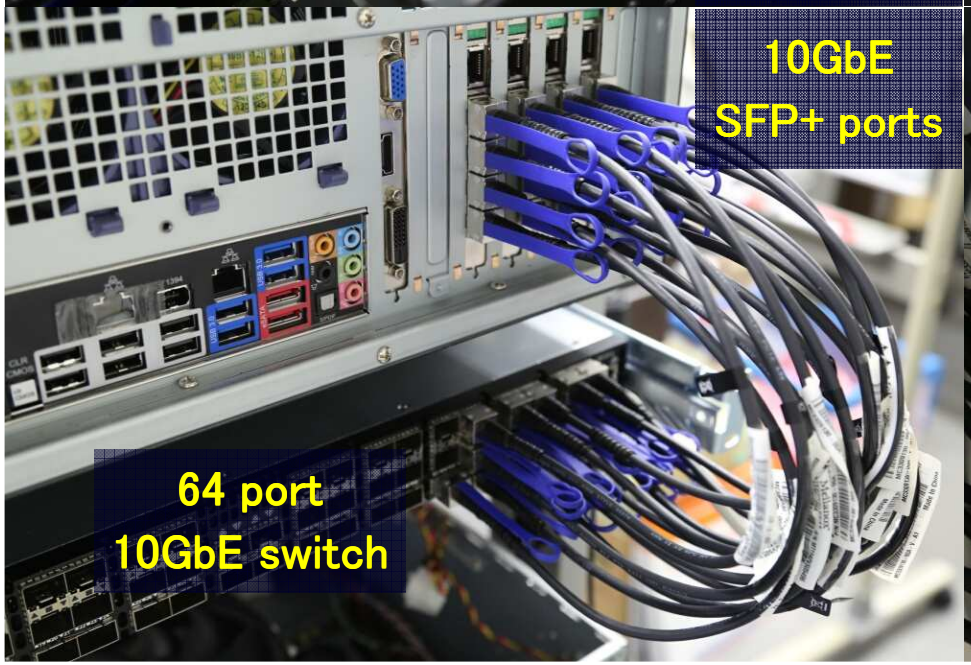
More Photos



4 FPGAs on node

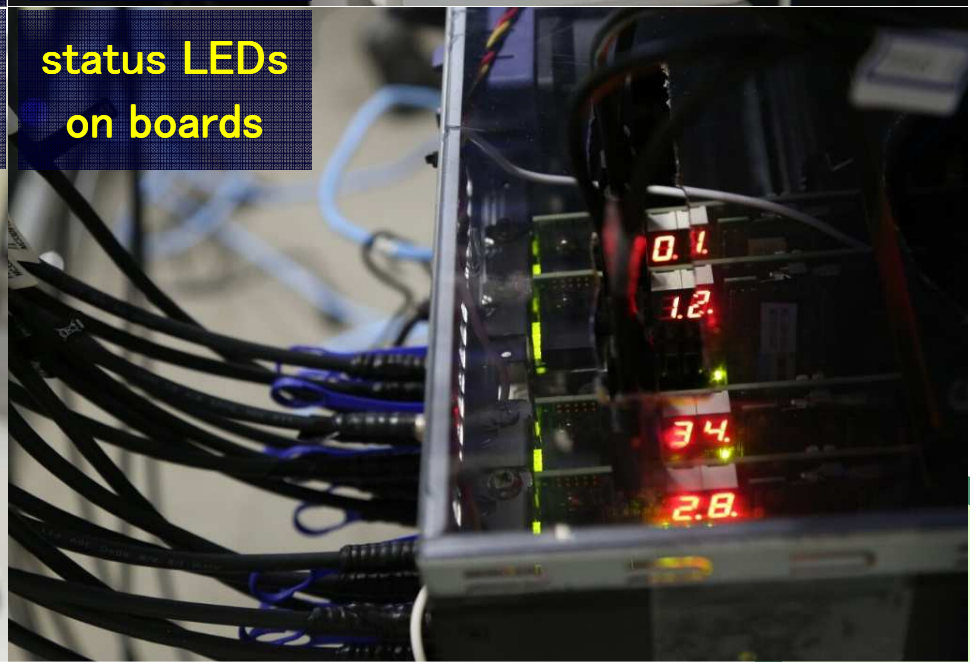


Temperature sensors



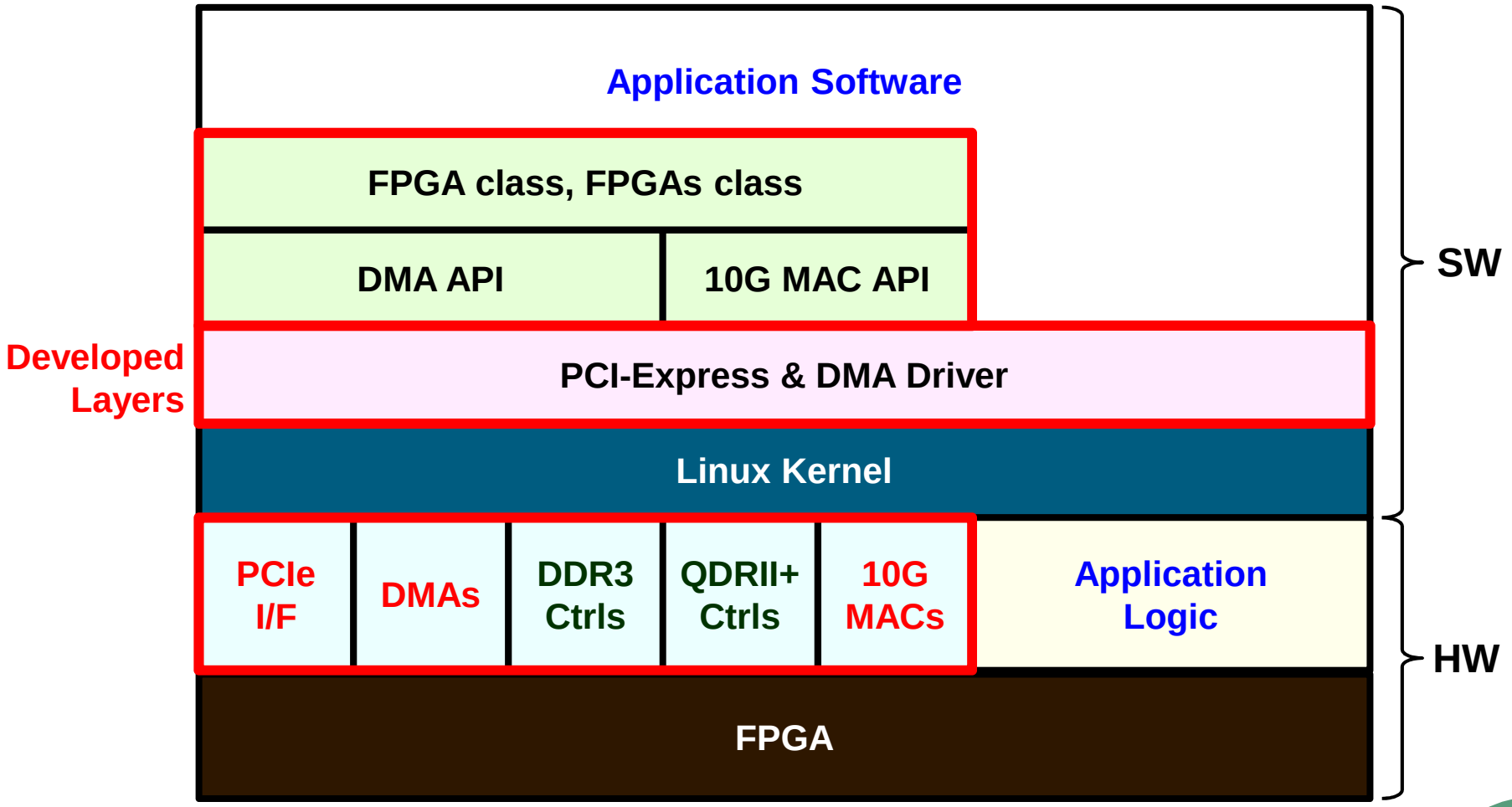
10GbE SFP+ ports

64 port 10GbE switch

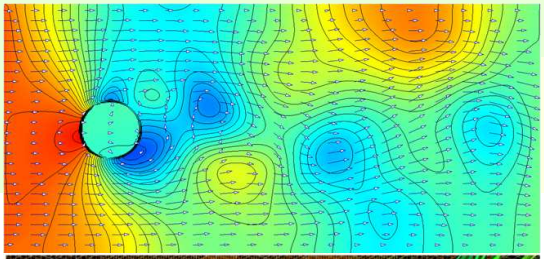


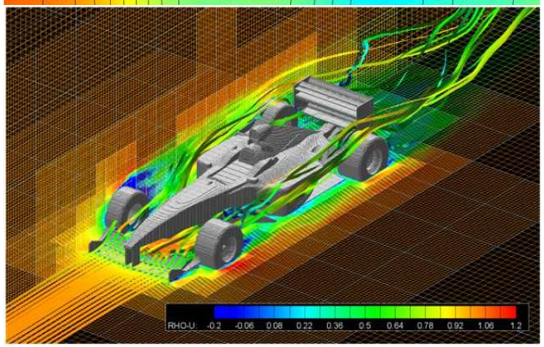
status LEDs on boards

Hardware/Software Stack

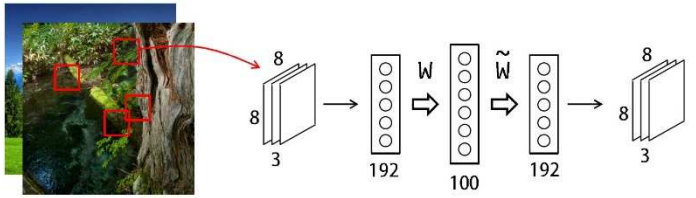


Future Work





- **Scalable and low-power computation**
  - ✓ Parallel fluid simulation with building cube method
  - ✓ Deep learning for image/video recognition
  - ✓ Molecular dynamics simulation
  - ✓ Gene info processing



- **Further development of framework**
  - ✓ Partial reconfiguration support
  - ✓ FPGA-direct communication via PCIe
  - ✓ Inter FPGA communication with SATA cables
  - ✓ Remote DMA among FPGAs

- **System tools**
  - ✓ OS management of FPGA resources
  - ✓ Stream processor generator : SPGen