Custom Computing with Reconfigurable Technologies for Efficient Acceleration of CFD Kernels

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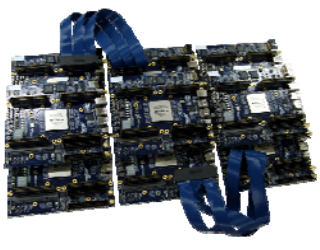
Outline

- **Why Custom Computing?**
- **FPGA-based Stream Processor**
- **FPGA-based Real-time Data Compressor**
- **Summary**

FPGA-based data-compressor



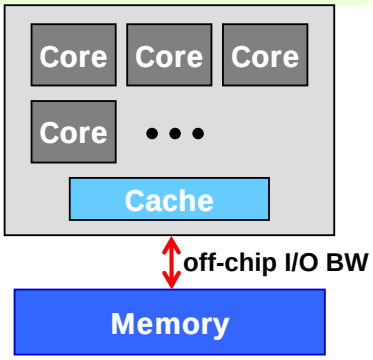
FPGA-based stream processor

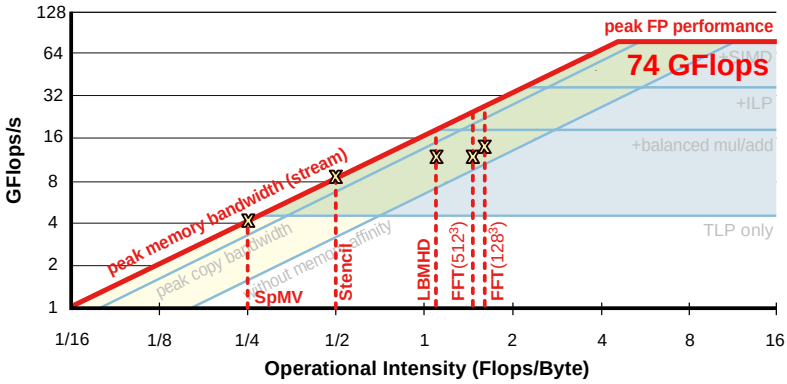
Introduction

General-purpose μ-processors

Increased cores, but
low growing rate of off-chip I/O bandwidth

- ✓ Gap between the memory bandwidth and the peak arithmetic performance
- ✓ Only a fraction of the peak performance





Roof line model of two AMD OpteronX4

Samuel Williams, Andrew Waterman and David Patterson, "Roofline: An Insightful Visual Performance Model for Multicore Architectures," Comm. of ACM, Vol.52, No.64, 65-76, 2009.

Introduction

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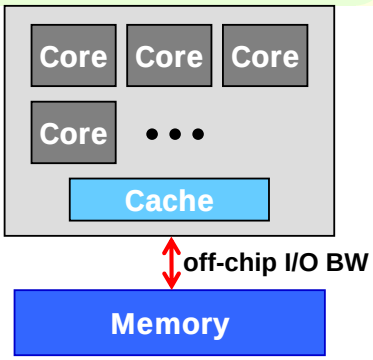


Their massively-parallel systems

- ✓ Communication overhead
- ✓ Limited scalability
- ✓ Very inefficient computation

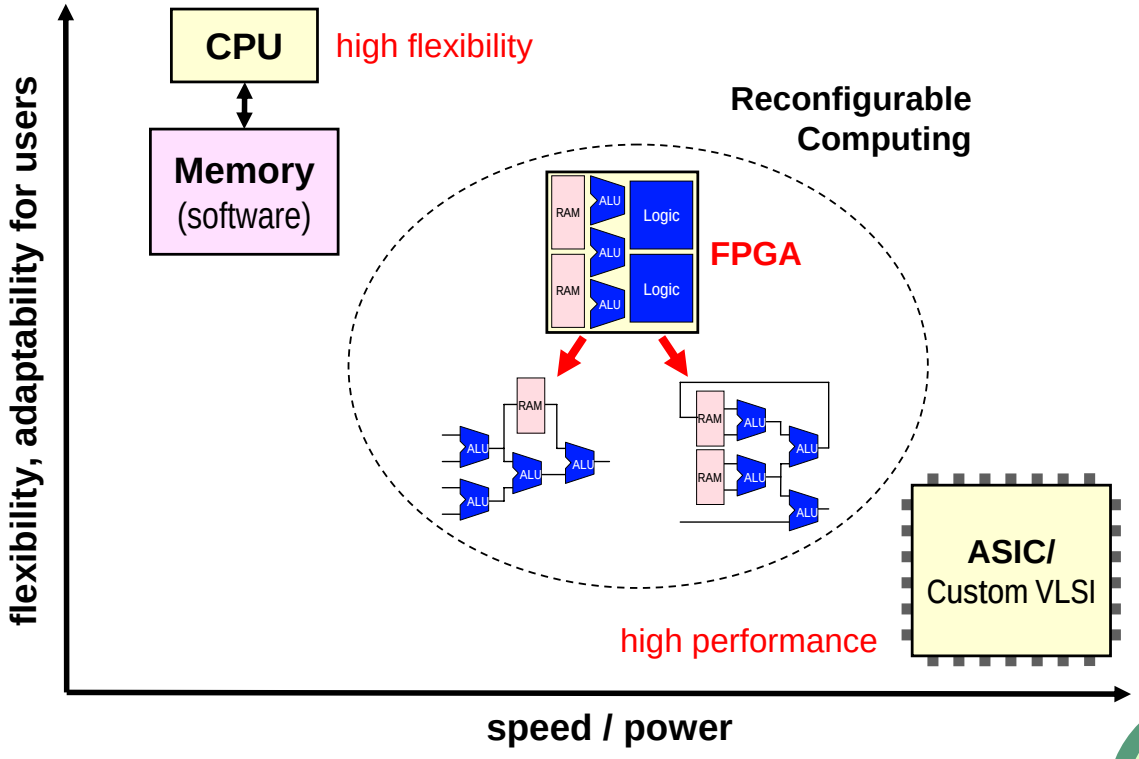
... a few % of the peak GFlops of an entire large-scale system

If we give resource-balanced HW adaptively to each application, happy? YES!

But how?

Custom Computing Machine!

Platform for Custom Computing Machines

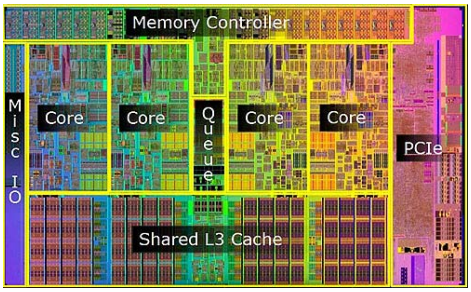


What's FPGA (Field-Programmable Gate Array) ?

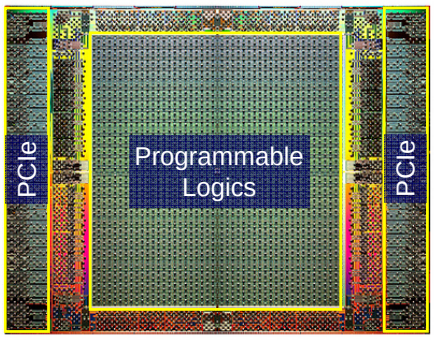
Core i7 processor

Stratix IV FPGA

What's FPGA (Field-Programmable Gate Array) ?



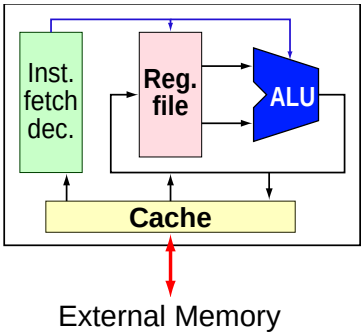
Die photo of Core i7 processor

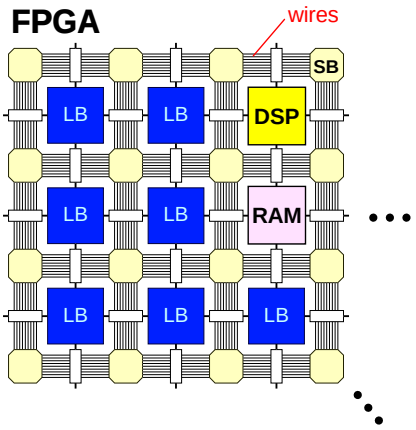


Die photo of Stratix IV FPGA

What's FPGA (Field-Programmable Gate Array) ?

Microprocessor (each core)





Components for program execution:

- ✓ register files
- ✓ ALUs (data-paths)
- ✓ control logic
- ✓ cache memory

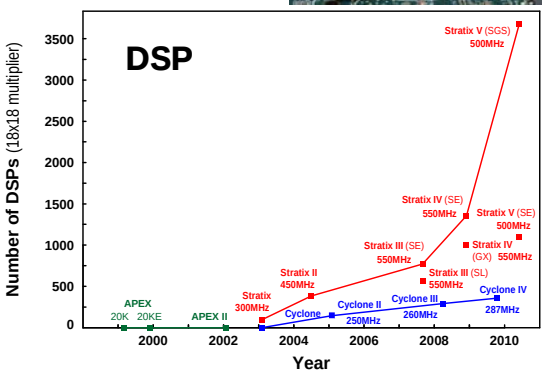
Components to make logics:

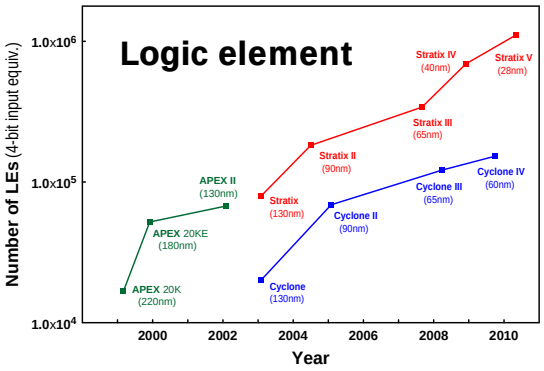
- ✓ logic blocks (LBs)
- ✓ DSP blocks (integer comput.)
- ✓ block RAMs
- ✓ wires & switch-blocks (SBs)

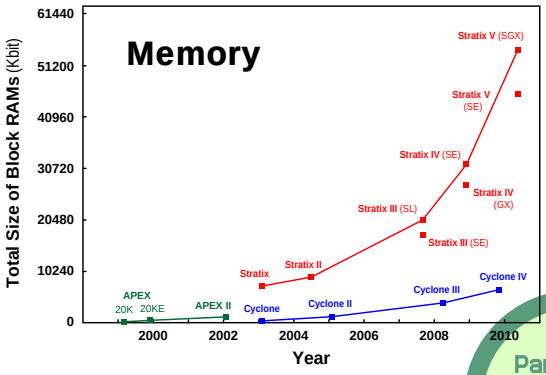
FPGA's Potential for HPC

State-of-the-art FPGAs

- ✓ Reconfigurable commodity device
- ✓ Larger & faster
- ✓ Lower initial-cost than VLSIs
- ✓ High potential for custom computing with floating-point operations

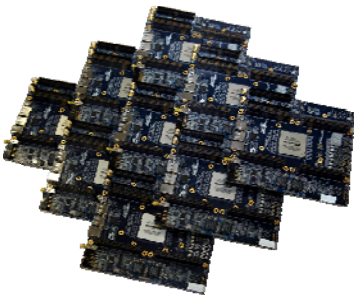




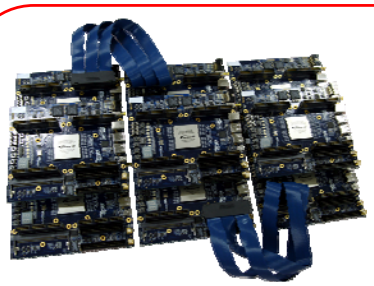


Our Approaches toward Custom HPC

FPGA-based custom machines with tailored structures for app. specific computing and memory



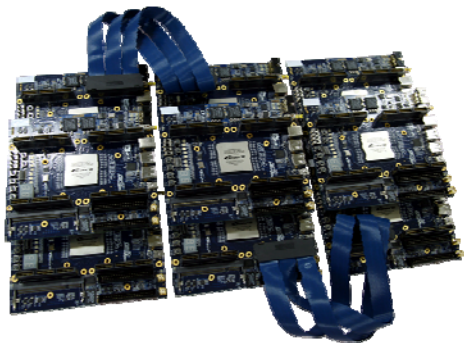
Systolic-array processor
for finite difference method

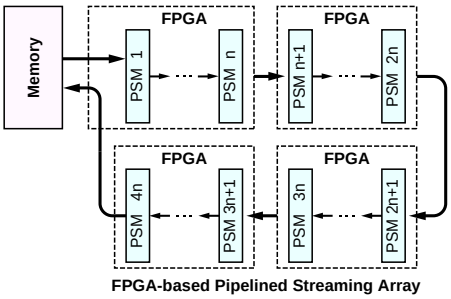


Stream processor with extensible custom pipelines

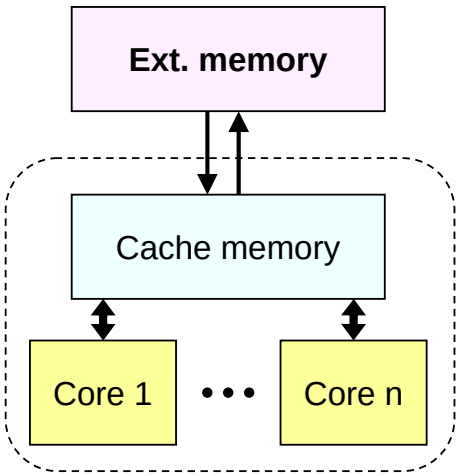
Real-time numerical data compressor for improving memory bandwidth

Stream Processor with Extensible Custom Pipelines for CFD Kernels





Problem of Many-Core Processors



Many cores require many data.

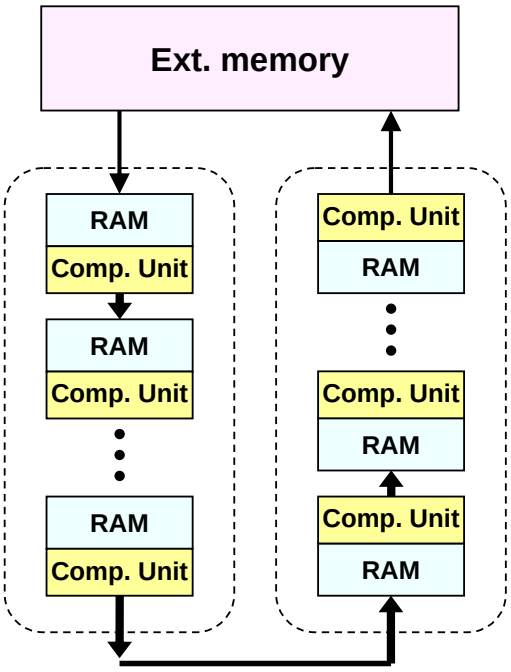
but

Insufficient memory bandwidth

↓

Cores are not fully utilized, resulting in low scalability.

Custom Machine with Stream Computing



Computing unit requires only the outputs of the previous unit

↓

All units can operate with the constant bandwidth.

More units, higher performance.

What kind of kernels can be streamed?

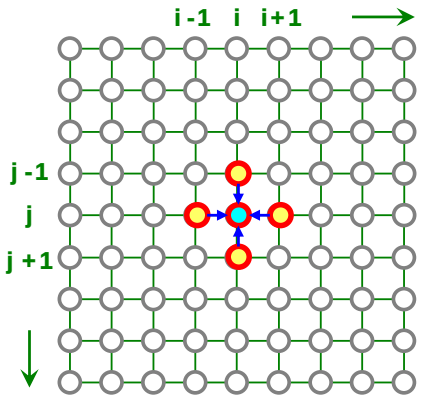
Time-Marching Stencil Computation

```
for (n=0; n< N_max ; n++)   <-- Time marching
  for (j=0; j< J_max ; j++)
    for (i=0; i< I_max ; i++)
      v'_i,j = f (v_i,j , v_i+1,j , v_i-1,j , v_i,j+1 , v_i,j-1)
```

Grid traverse

Stencil computation

2D Time-marching Stencil Computation



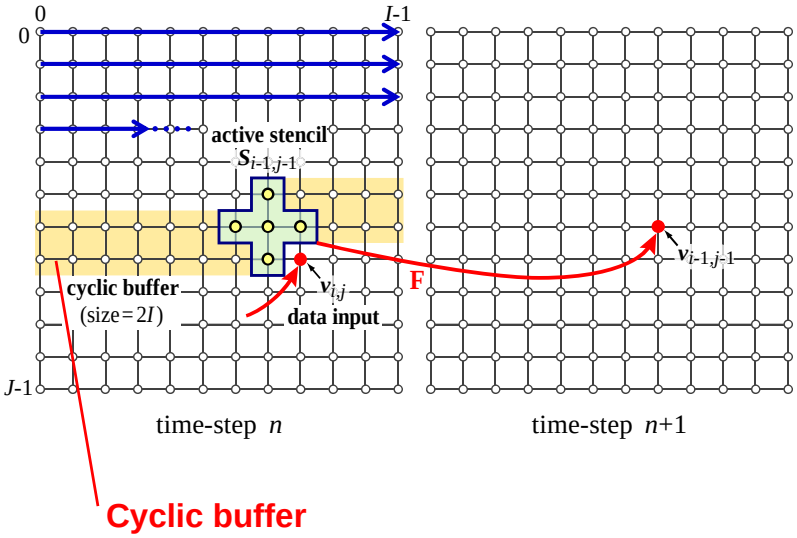
Computational grid

Stencil Computation

- ✓ Update all the grid-points with local stencil computation
- ✓ Repeat them for time-marching

(Examples: Jacobi computation, LGM, LBM)

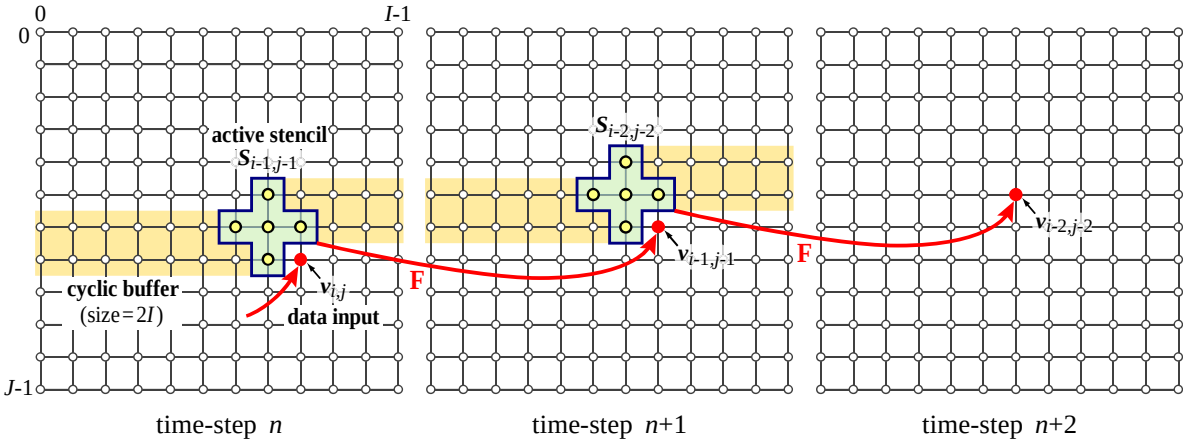
Make It Stream!



Cyclic buffer

Tomoyoshi Kobori and Tsutomu Maruyama, "A High Speed Computation System for 3D FCHC Lattice Gas Model with FPGA," Proceedings of FPL2003, 755-765, 2003.

Make It Stream!



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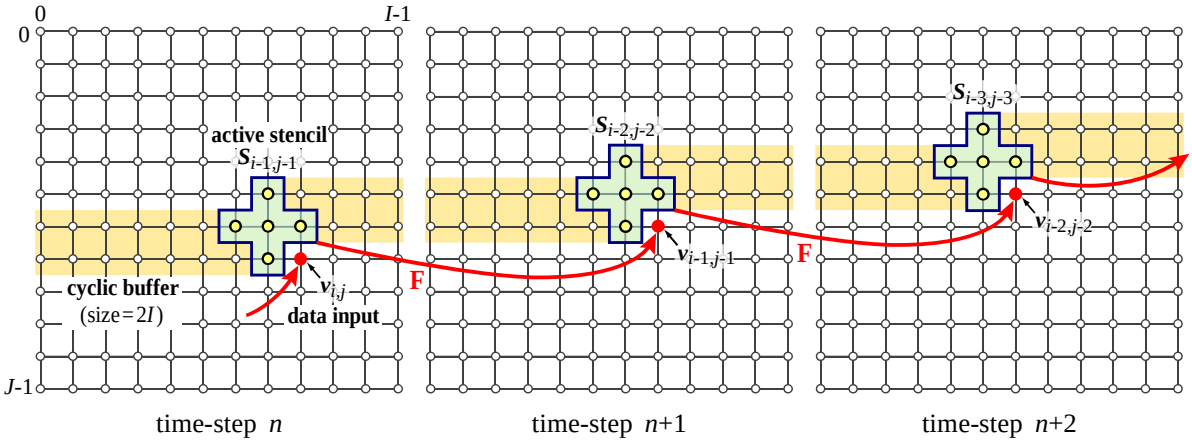
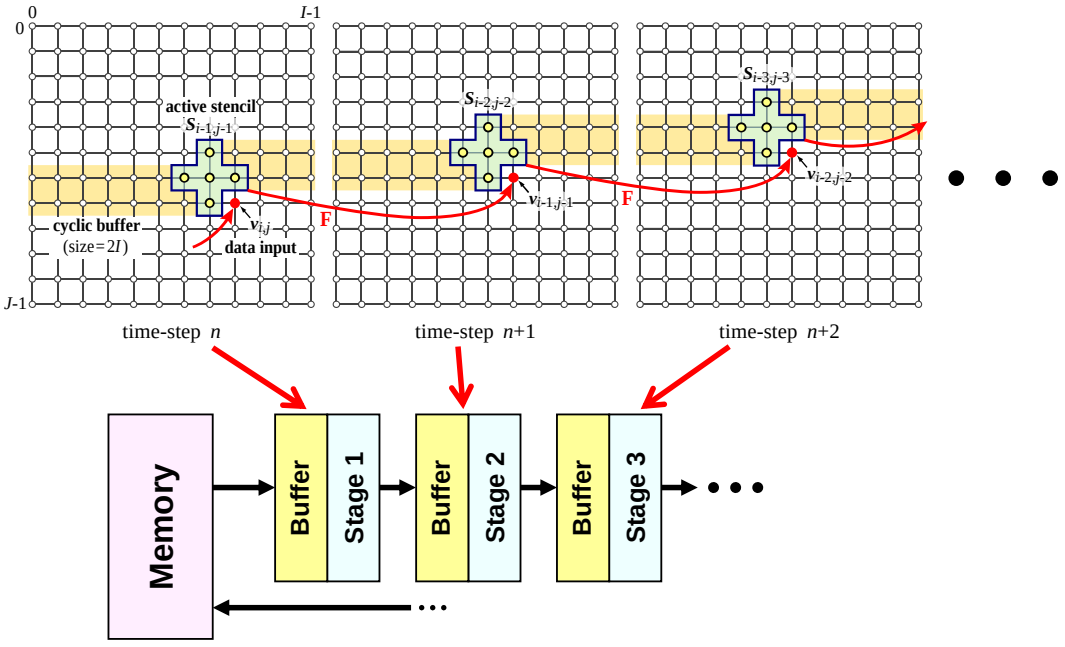


Pipelined execution of streamed multiple time-steps

Required bandwidth is constant!

Tomoyoshi Kobori and Tsutomu Maruyama, "A High Speed Computation System for 3D FCHC Lattice Gas Model with FPGA," Proceedings of FPL2003, 755-765, 2003.

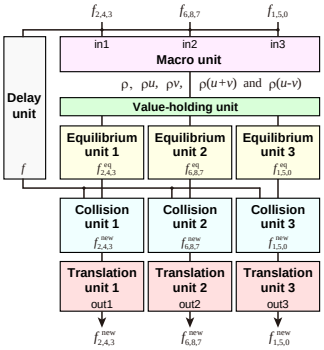
Stream Processor w/ Extensible Stages



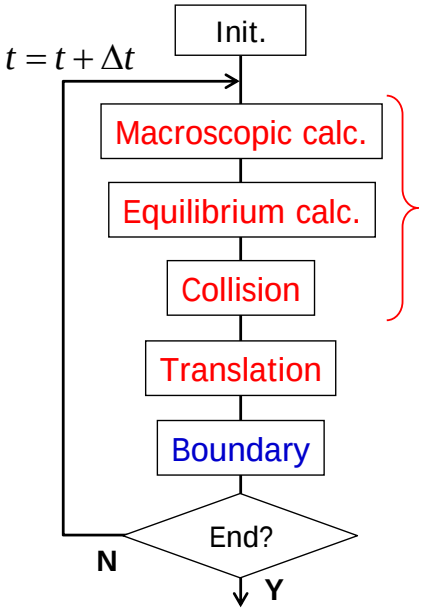
Multiple-stage execution with one memory-read.

Single-Stage Stream Processor for Lattice Boltzmann Method (LBM)

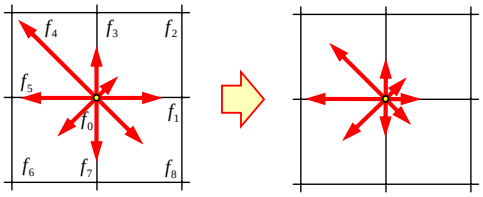
FPGA board



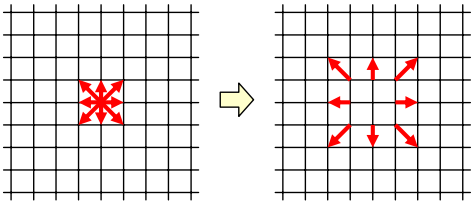
Algorithm for LBM



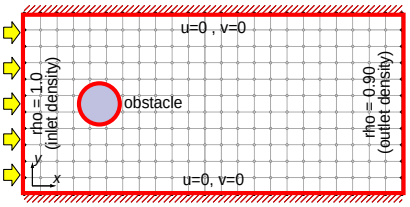
Relaxation to locally equilibrium state



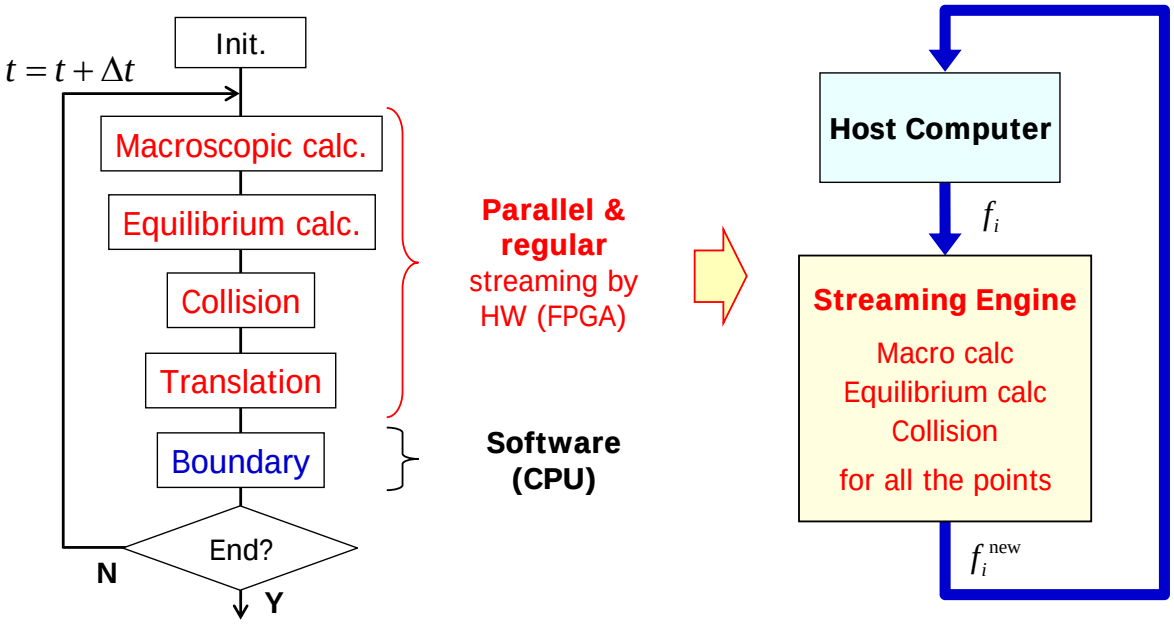
Diffuse particles



Boundary condition



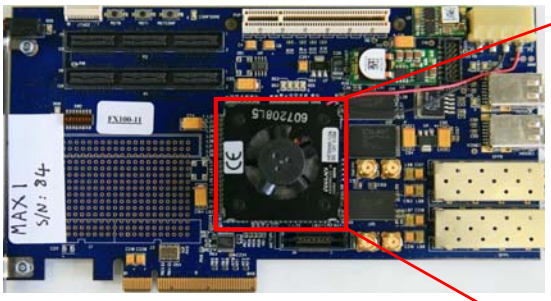
Design of Pipeline Stage Unit



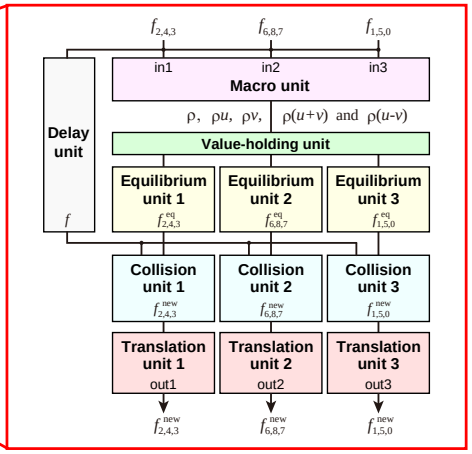
Streaming by FPGA

Kentaro Sano, et al., "FPGA-based Streaming Computation for Lattice Boltzmann Method,"
Procs of the International Conference on Field-Programmable Technology, pp.233-236, 2007.

Implementation of Single Stage



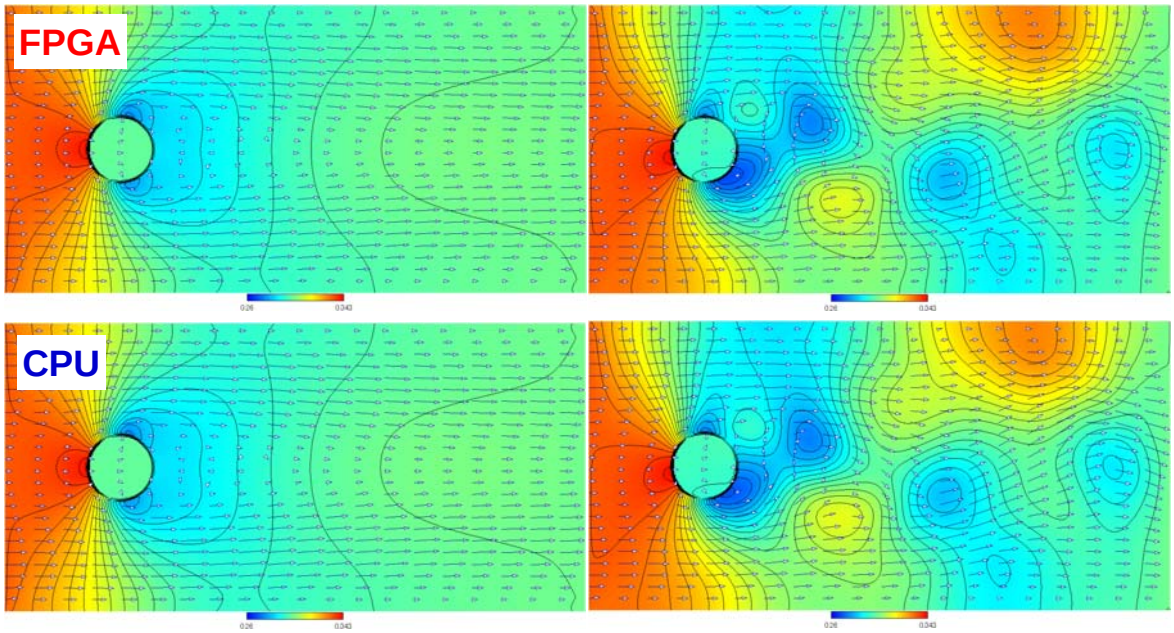
Xilinx Virtex4 FPGA (2005)



Single stage of streaming LBM
(operating at **100MHz**)

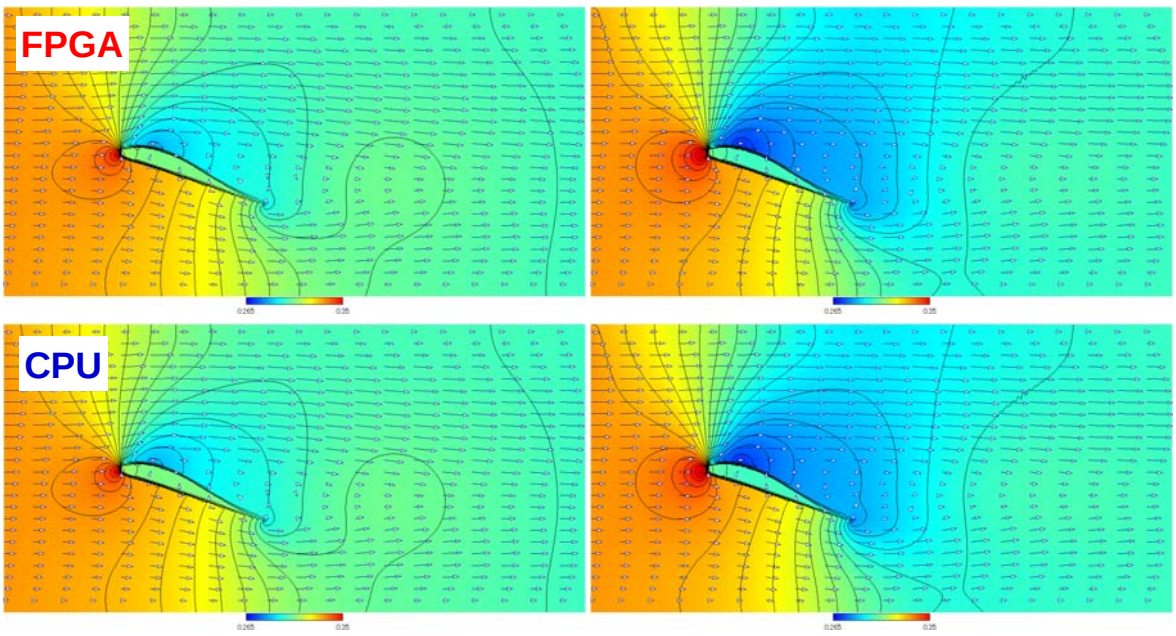
Real-time 2D LBM computation by FPGA

Computed Results (Circle, RE=300)



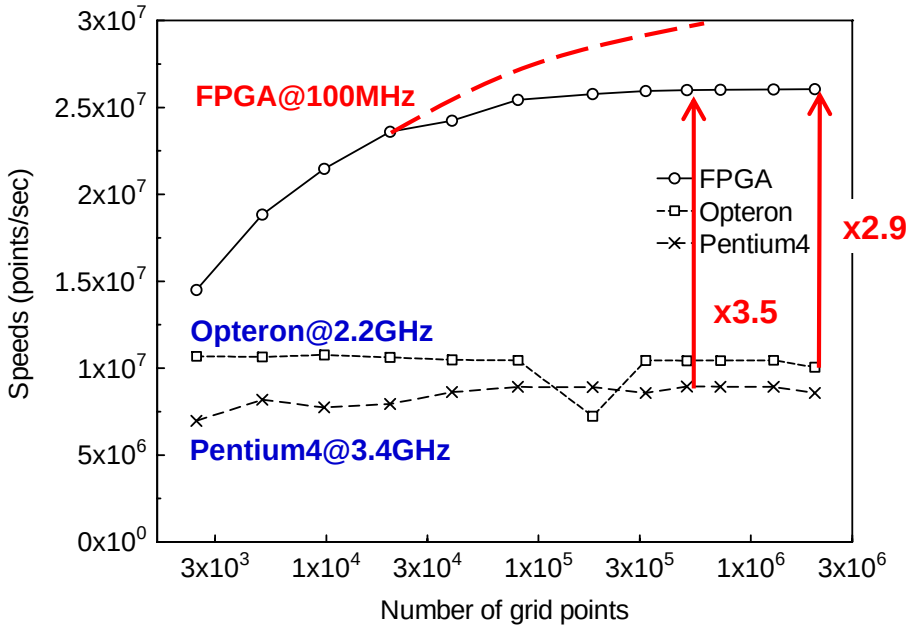
T=10000 T=50000

Computed Results (Wing, RE=300)



T=4000 T=50000

Speedup by Single Stage



***n* stages**
⇒ x 3*n*

Bandwidth of PCI-Express limits the performance.

Real-time Data Compressor to Improve Memory Bandwidth for Streamed CFD Kernels

FPGA-based data compressor

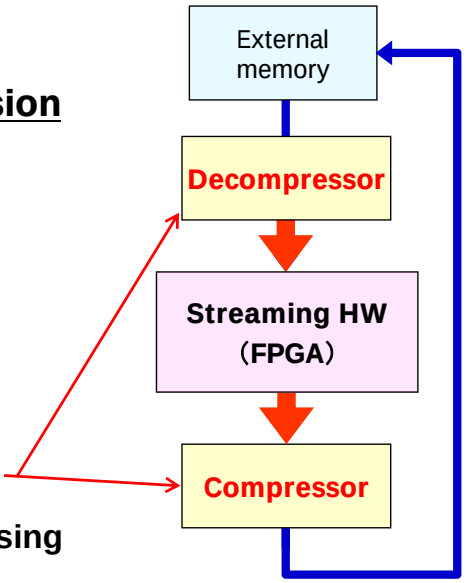
Strategy

Bandwidth enhancement for stream computing by data compression

- ✓ **Lossless compression** of floating-point (FP) data streams
- ✓ **Only high-throughput** required (Stream comp. is tolerant to latency.)

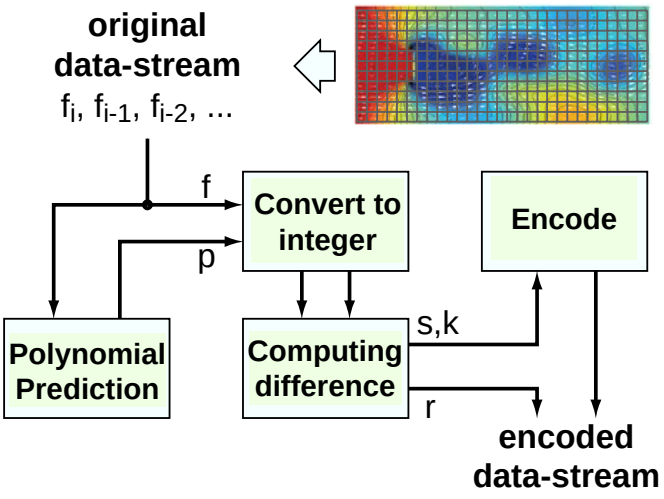
FPGA-based compression hardware

- ✓ High-throughput by **hardware processing**
- ✓ **Compact circuit** that can be attached to memory-I/F unit



Stream Computing

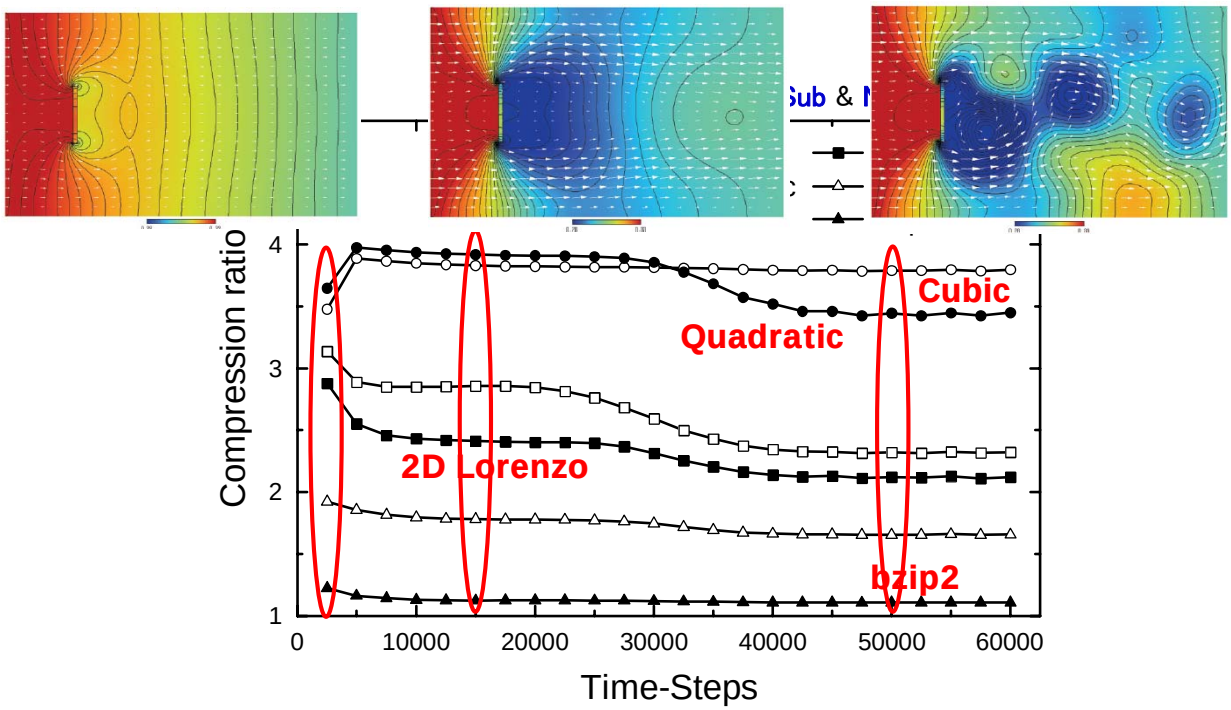
Compression with Polynomial Prediction



Overview of compression algorithm

More accurate prediction gives integer-difference closer to zero, which can be recorded with fewer bits.

Compression Ratios for 2D LBM Case

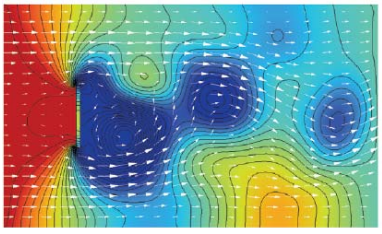


We estimate x4 wider bandwidth on average.

Summary

- **FPGA-based custom computing**
  - ✓ Why we focus on?
  - ✓ How good expected to be?

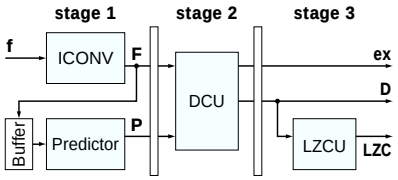
- **Stream processor with extensible stages**
  - ✓ Higher scalability with slow memory
  - ✓ 2D LBM example



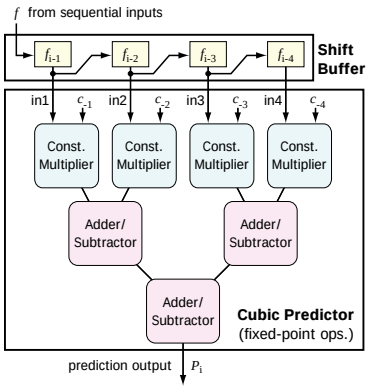
- **Data compression for wider BW**
  - ✓ Prediction-based compression
  - ✓ 4 x Compression = 4 times faster memory!

Future Directions of Custom Computing

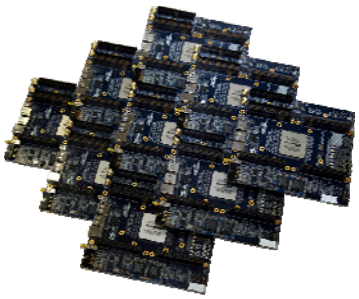
- **Performance issues**
  Further exploration required on
  - ✓ Algorithm level
  - ✓ Architecture level
  - ✓ Circuit level
- **Productivity issues**
  - ✓ Programming/Design tools
  - ✓ Standards for programming, OS, HW
  - ✓ Costs
- **Future work**
  - ✓ Prototype implementation & evaluation
  - ✓ Developing tools for HW and SW design (HW compiler for SW codes, etc.)



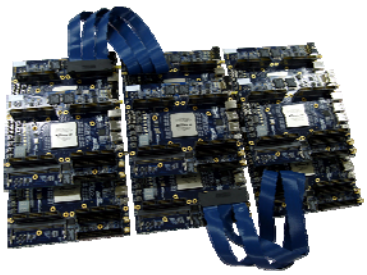
Design of 3-stage compressor



Design of cubic predictor



Systolic-array processor



Stream processor

Thank you!

Real-time data compressor